WHAT IS CLAIMED IS:

1. A method of testing a serial transceiver chip for jitter tolerance, the transceiver including at least one transmitter and at least one receiver, the method comprising:

generating a serialization clock;

adding one or more known and controlled amount of jitter to the serialization clock;

transmitting a known sequence of test signals using the serialization clock with the added jitter;

causing a clock and data recovery mechanism in a receiver to recover the test signals; and

comparing the recovered test signals with said known sequence of test signals thereby testing the ability of the clock and data recovery mechanism to tolerate the jitter that was added;

wherein the steps of generating a serialization clock, adding one or more known and controlled amount of jitter to the serialization clock, transmitting a known sequence of test signals using the serialization clock with the added jitter, and causing a clock and data recovery mechanism in the receiver to recover the test signals with jitter are all performed inside the serial transceiver chip.

2. The method of claim 1 wherein the known sequence of test signals is created by a PRBS (Pseudo Random Binary Sequence) generation mechanism and wherein comparing the recovered test signals is done by use of the PRBS verification mechanism.

3. The method of claim 2 wherein creating the known sequence of test signals and comparing the recovered sequence of test signals is performed inside the serial transceiver chip.

4. The method of claim 1 wherein the known sequence of test signals is created inside the serial transceiver chip and wherein comparing the recovered sequence of test signals is also performed inside the serial transceiver chip.

5. The method of claim 1 wherein adding one or more known and controlled amount of jitter is performed by use of an interpolator and an interpolator control mechanism programmed to create the known and controlled amount of jitter.

6. The method of claim 5 wherein the known sequence of test signals is created by a PRBS (Pseudo Random Binary Sequence) generation mechanism and wherein comparing the recovered test signals is done by use of the PRBS verification mechanism.

7. The method of claim 6 wherein creating the known sequence of test signals and comparing the recovered sequence of test signals is performed inside the serial transceiver chip.

8. The method of claim 5 wherein the known sequence of test signals is created inside the serial transceiver chip and wherein comparing the recovered sequence of test signals is also performed inside the serial transceiver chip.

9. A method of testing a serial receiver for jitter tolerance, the serial receiver being fully contained on a single semiconductor substrate, the method comprising:

generating a known sequence of test signals containing negligible jitter relative to a local reference clock;

causing a clock and data recovery mechanism in the serial receiver to recover the test signals;

adding one or more known and controlled amount of jitter into the clock recovery mechanism to force the clock recovery mechanism to compensate for the added jitter; and

comparing the recovered test signals with said known sequence of test signals thereby testing the ability of the clock and data recovery mechanism to tolerate the jitter that was added;

wherein the steps of causing a clock and data recovery mechanism in the receiver to recover the test signals, and adding the known and controlled amount of jitter to the clock recovery mechanism are all performed inside the serial receiver.

10. The method of claim 9 wherein the known sequence of test signals is created by a PRBS (Pseudo Random Binary Sequence) generation mechanism and wherein comparing the recovered test signals is done by use of a PRBS verification mechanism.

11. The method of claim 10 wherein comparing the recovered sequence of test signals is performed inside the serial receiver.

12. The method of claim 9 wherein comparing the recovered sequence of test signals is performed inside the serial receiver.

13. The method of claim 9 wherein adding one or more known and controlled amount of jitter is performed by use of an interpolator control mechanism programmed to create the known and controlled amount of jitter.

14. The method of claim 13 wherein the known sequence of test signals is created by a PRBS (Pseudo Random Binary Sequence) generation mechanism and wherein comparing the recovered test signals is done by use of a PRBS verification mechanism.

15. The method of claim 14 wherein comparing the recovered sequence of test signals is performed inside the serial receiver.

16. The method of claim 13 wherein comparing the recovered sequence of test signals is performed inside the serial receiver.

17. A method of testing a serial transceiver for jitter transfer, the serial transceiver including at least one transmitter and at least one receiver, the serial transceiver being fully contained on a single semiconductor substrate, the method comprising:

generating a serialization clock;

adding one or more known and controlled amounts of jitter to the serialization clock;

transmitting a sequence of test signals using the serialization clock with the added jitter;

causing a clock and data recovery mechanism in a receiver to recover a clock signal from the transmitted sequence of test signals;

monitoring and measuring an amount of jitter present in the recovered clock signal; and

comparing jitter present in the recovered clock with jitter added to the serialization clock thereby testing the jitter transfer characteristic of the transceiver;

wherein the steps of generating a serialization clock, adding jitter to the serialization clock, transmitting a sequence of test signals, monitoring and measuring an amount of jitter in the recovered clock signal, and comparing jitter present in the recovered clock with jitter added to the serialization clock are all performed inside the serial transceiver.

18. The method of claim 17 wherein adding one or more known and controlled amounts of jitter is performed by use of an interpolator and an interpolator control mechanism programmed to create the known and controlled amounts of jitter.

19. The method of claim 17 wherein monitoring and measuring the amount of jitter present in the recovered clock signal is performed by use of an up/down counter that is responsive to direction and step control signals for an interpolator used for clock recovery, and wherein comparing the jitter present in the recovered clock signal is performed by use of a programmable

comparator set to issue a warning if a maximum count achieved by an up/down counter exceeds the maximum allowed to pass the transfer test.

20. The method of claim 17 wherein:

adding one or more known and controlled amounts of jitter is performed by use of an interpolator and an interpolator control mechanism programmed to create the known and controlled amounts of jitter;

monitoring and measuring the amount of jitter present in the recovered clock signal is performed by use of an up/down counter that is responsive to direction and step control signals for the interpolator used for clock recovery;

comparing jitter present in the recovered clock with jitter added to the serialization clock is performed by use of a programmable comparator that is set to issue a warning if a maximum count achieved by an up/down counter exceeds a maximum allowed to pass a transfer test.

21. The method of claim 20 wherein the sequence of test signals are generated on the single semiconductor substrate that also contains the transceiver.

22. The method of claim 17 wherein the sequence of test signals are generated on the single semiconductor substrate that also contains the transceiver.

23. A method of testing a serial receiver for jitter transfer, the serial receiver being fully contained on a single semiconductor substrate, the method comprising:

generating a sequence of test signals containing negligible jitter relative to a local reference clock;

causing a clock recovery mechanism in the serial receiver to recover a clock signal from the sequence of test signals, the clock recovery mechanism contained on the single semiconductor substrate;

adding one or more known and controlled amounts of jitter into the clock recovery mechanism to force the clock recovery mechanism to compensate for added jitter;

monitoring and measuring an amount of activity in the clock recovery mechanism; and

comparing the amount of activity in the clock recovery mechanism with an expected amount of activity that is based on the jitter added thereby testing a jitter transfer characteristic of the receiver;

wherein the steps of adding one or more known and controlled amounts of jitter into the clock recovery mechanism, monitoring and measuring an amount of activity in the clock recovery mechanism, and comparing the amount of activity in the clock recovery mechanism with an expected amount of activity are all performed inside the serial receiver.

24. The method of claim 23 wherein adding one or more known and controlled amounts of jitter is performed by use of an interpolator control mechanism that is programmed to create the known and controlled amounts of jitter.

25. The method of claim 24 wherein monitoring and measuring the amount of activity in the clock recovery mechanism is performed by use of an up/down counter that is responsive to

direction and step control signals for an interpolator used for clock recovery, and wherein comparing the amount of activity in the clock recovery mechanism with the expected amount of activity is performed by use of a programmable comparator set to issue a warning if a maximum count achieved by an up/down counter exceeds the maximum allowed to pass the transfer test.

26. The method of claim 23 wherein monitoring and measuring the amount of activity in the clock recovery mechanism is performed by use of an up/down counter that is responsive to direction and step control signals for an interpolator used for clock recovery, and wherein comparing the amount of activity in the clock recovery mechanism with the expected amount of activity is performed by use of a programmable comparator set to issue a warning if a maximum count achieved by an up/down counter exceeds the maximum allowed to pass the transfer test.

27. The method of claim 26 wherein the sequence of test signals are generated on the single semiconductor substrate that also contains the receiver.

28. The method of claim 23 wherein the sequence of test signals are generated on the single semiconductor substrate that also contains the receiver.

29. A method of testing a FIFO (First In First Out) circuit on a single semiconductor substrate, the method comprising:

generating an on-chip clock at the same frequency as a reference clock;

incrementally adding a known and controlled amount of phase shifts to the on-chip clock signal;

using the reference clock and the phase-shifted on-chip clock to drive the FIFO circuit; and

measuring an amount of phase-shift that can be added to the on-chip clock signal before the FIFO experiences overflow and/or underflow errors;

wherein the steps of generating an on-chip clock, incrementally adding a known and controlled amount of phase shifts, using the reference clock and the phase-shifted on-chip clock to drive the FIFO circuit, and measuring an amount of phase-shift are all performed on the single semiconductor substrate.

30. The method of claim 29 and further comprising:

providing a PRBS pattern to be used as input data for the FIFO; and

checking output data from the FIFO with a PRBS verifier, the PRBS verifier being disposed on the single semiconductor substrate.

31. The method of claim 30 wherein the PRBS pattern is provided by an on-chip PRBS generator clocked by the reference clock signal.

32. The method of claim 29 wherein incrementally adding a known and controlled amount of phase shifts is performed by use of an interpolator and an interpolator control mechanism programmed to create desired phase shifts.

33. The method of claim 32 and further comprising:

providing a PRBS pattern to be used as input data for the FIFO; and

checking output data from the FIFO with a PRBS verifier, the PRBS verifier being disposed on the single semiconductor substrate.

34. The method of claim 33 wherein the PRBS pattern is provided by an on-chip PRBS generator clocked by the reference clock signal.

35. A built-in self-test (BIST) apparatus for jitter tolerance for use on a serial transceiver, the serial transceiver including one or more transmitters and one or more receivers disposed on a single semiconductor substrate, the BIST apparatus comprising:

a serialization clock generator for generating a serialization clock;

a mechanism for adding one or more known and controlled amounts of jitter to the serialization clock;

a transmitter that uses the serialization clock with added jitter to transmit a known sequence of test signals;

a clock and data recovery mechanism in a receiver to recover the test signals; and

a bit stream verification mechanism used to verify that the recovered test signals match the known sequence of test signals thereby determining whether the clock and data recovery mechanism can tolerate the jitter that was added;

wherein the serialization clock generator, the mechanism for adding jitter, the transmitter, and the clock and data recovery mechanism are also disposed on the single semiconductor substrate.

36. A built-in self-test (BIST) apparatus for jitter tolerance for use on a serial transceiver, the serial transceiver including one or more transmitters and one or more receivers disposed on a single semiconductor substrate, the BIST apparatus comprising:

means for generating a serialization clock, the means for generating being disposed on the single semiconductor substrate;

means for adding one or more known and controlled amounts of jitter to the serialization clock, the means for adding being disposed on the single semiconductor substrate;

means for using the serialization clock with added jitter to transmit a known sequence of

test signals, the means for using being disposed on the single semiconductor substrate;

means for recovering the test signals, the means for recovering being disposed on the single semiconductor substrate; and

means for verifying that the recovered test signals match the known sequence of test signals, the means for verifying being disposed on the single semiconductor substrate.

37. A built-in self-test (BIST) apparatus for jitter tolerance for use on a serial receiver, the serial receiver being disposed on a single semiconductor substrate, the BIST apparatus comprising:

a sequential test signal generator to apply a known sequence of test signals that contain negligible jitter relative to a local reference clock to the receiver;

a clock and data recovery mechanism in the receiver to recover the test signals, the clock and data recovery mechanism being disposed on the single semiconductor substrate;

a mechanism to add one or more known and controlled amount of jitter into the clock recovery mechanism which cause the clock recovery mechanism to compensate for the added jitter, the mechanism to add jitter being disposed on the single semiconductor substrate; and

a bit stream verification mechanism used to verify that the recovered test signals match the known test signals thereby confirming that the clock and data recovery mechanism can tolerate the jitter that was added.

38. A built-in self-test (BIST) apparatus for jitter tolerance for use on a serial receiver, the serial receiver being disposed on a single semiconductor substrate, the BIST apparatus comprising:

means for applying a known sequence of test signals that contain negligible jitter relative

to a local reference clock to the receiver;

means for recovering the clock and data contained in the test signals, the means for recovering being disposed on the single semiconductor substrate;

means for adding one or more known and controlled amount of jitter into the clock recovery mechanism which cause the clock recovery mechanism to compensate for the added jitter, the means for adding being disposed on the single semiconductor substrate; and

means for verifying that the recovered test signals match the known test signals thereby confirming that the clock and data recovery mechanism can tolerate the jitter that was added.

39. A built-in self-test (BIST) apparatus for jitter transfer for use on a serial transceiver, the serial transceiver including at least one transmitter and at least one receiver disposed on a semiconductor substrate, the BIST apparatus comprising:

a serialization clock generator to generate a serialization clock, the serialization clock generator being disposed on the semiconductor substrate;

a mechanism for adding one or more known and controlled amount of jitter to the serialization clock, the mechanism for adding being disposed on the semiconductor substrate;

a transmitter that uses the serialization clock with the added jitter to transmit a sequence of test signals, the transmitter being disposed on the semiconductor substrate;

a clock and data recovery mechanism in a receiver to recover the test signals, the clock and data recovery mechanism being disposed on the semiconductor substrate;

a mechanism to monitor and measure the amount of jitter present in the recovered clock signal, the mechanism to monitor and measure being disposed on a semiconductor substrate; and

a mechanism to compare the jitter present in the recovered clock with the jitter added to

the serialization clock thereby testing the jitter transfer characteristic of the transceiver, the mechanism to compare being disposed on the semiconductor substrate.

40. A built-in self-test (BIST) apparatus for jitter transfer for use on a serial receiver, the serial receiver being fully contained on a single semiconductor substrate, the BIST apparatus comprising:

a signal generator to apply a sequence of test signals that contain negligible jitter relative to a local reference clock to the receiver;

a clock and data recovery mechanism in the receiver to recover the test signals, the clock and data recovery mechanism is disposed on the single semiconductor substrate;

a mechanism to add one or more known and controlled amounts of jitter into the clock recovery mechanism which cause the clock recovery mechanism to compensate for the added jitter, the mechanism to add jitter being disposed on the single semiconductor substrate;

a mechanism to monitor and measure the amount of activity in the clock recovery mechanism, the mechanism to monitor and measure being disposed on the single semiconductor substrate; and

a mechanism to compare the amount of activity in the clock recovery mechanism with the amount expected based on the jitter added thereby testing the jitter transfer characteristic of the receiver, the mechanism to compare being disposed on the single semiconductor substrate.

41. A built-in self-test (BIST) apparatus for jitter transfer for use on a serial receiver, the serial receiver being fully contained on a single semiconductor substrate, the BIST apparatus comprising:

means for applying a sequence of test signals that contain negligible jitter relative to a local reference clock to the receiver;

means for recovering clock and data contained in the test signals, the means for recovering being disposed on the single semiconductor substrate;

means for adding one or more known and controlled amounts of jitter into the clock recovery mechanism which cause the clock recovery mechanism to compensate for the added jitter, the means for adding jitter being disposed on the single semiconductor substrate;

means for monitoring and measuring the amount of activity in the clock recovery mechanism, the means for monitoring and measuring being disposed on the single semiconductor substrate; and

means for comparing the amount of activity in the clock recovery mechanism with the amount expected based on the jitter added thereby testing the jitter transfer characteristic of the receiver, the mechanism to compare being disposed on the single semiconductor substrate.

42. A built-in self-test (BIST) apparatus for a FIFO (First In First Out) circuit on a semiconductor substrate, the BIST apparatus comprising:

an on-chip clock generator capable of creating an on-chip clock signal with frequency that match the frequency of a reference clock;

a mechanism for adding known and controlled amount of phase shifts to the on-chip clock signal;

a FIFO circuit that has the reference clock and the phase shifting on-chip clock as inputs;

and

a mechanism that detects when the FIFO experiences overflow and/or underflow errors;

wherein the on-chip clock generator, the mechanism for adding known and controlled amount of phase shifts to the on-chip clock signal, the FIFO, and the mechanism that detects when the FIFO experiences overflow and/or underflow errors exist on the same semiconductor substrate.

43. An apparatus for inserting known and controlled amount of jitter onto a switching signal, the apparatus comprising:

an interpolator for inserting the jitter; and

an interpolator control mechanism programmed to create the desired jitter.